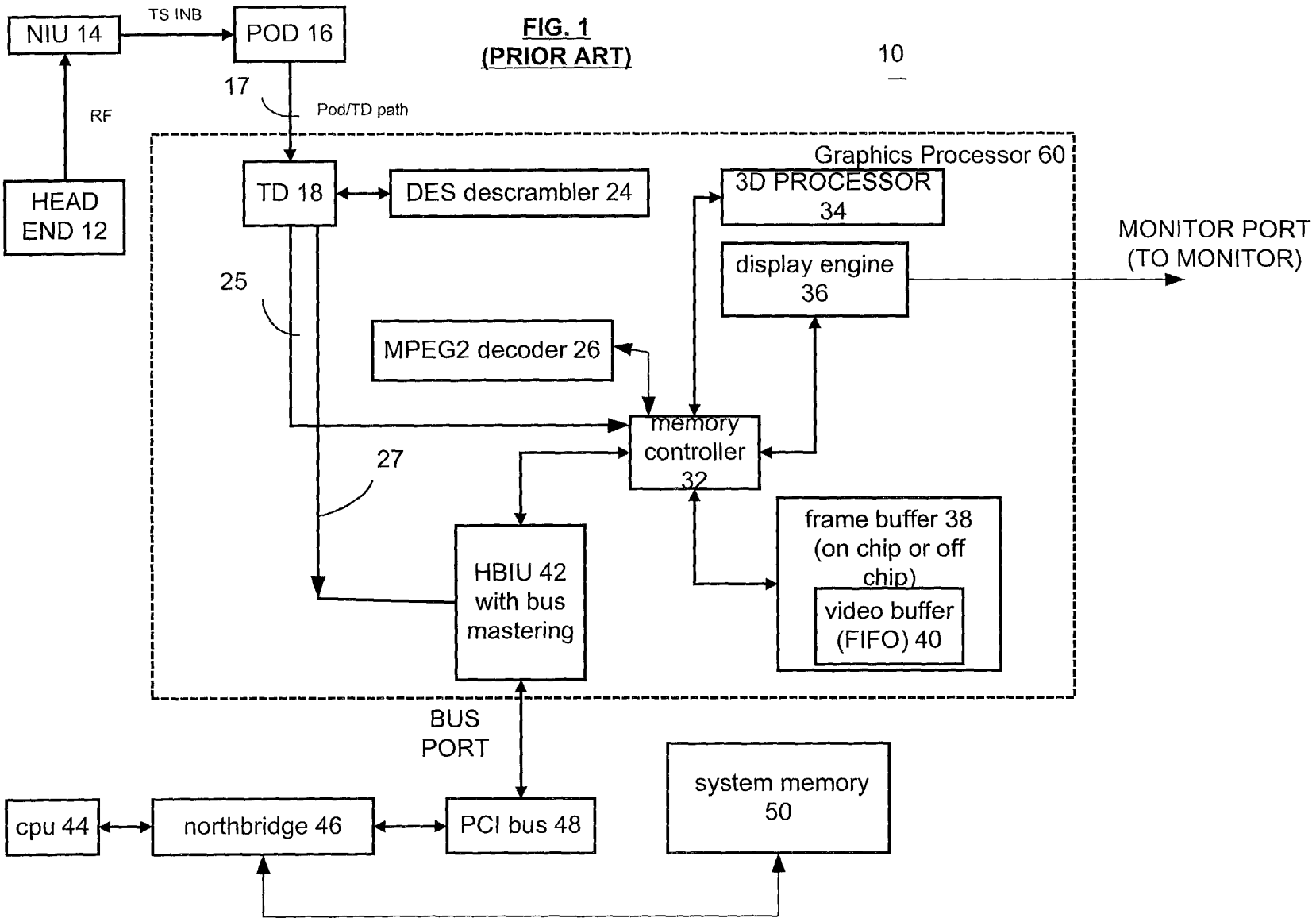


FIG. 1
(PRIOR ART)

10

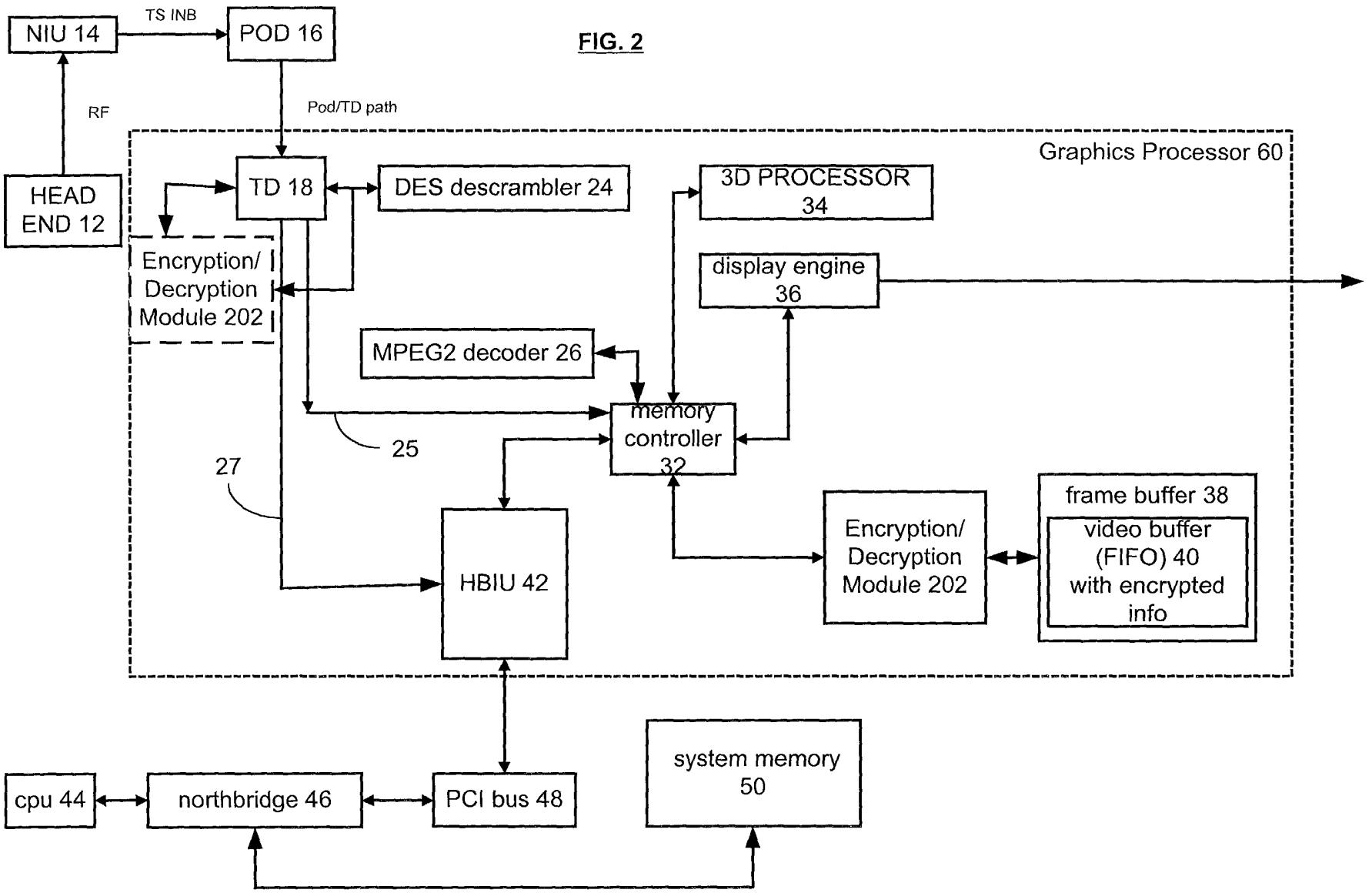


FIG. 2

FIG. 3

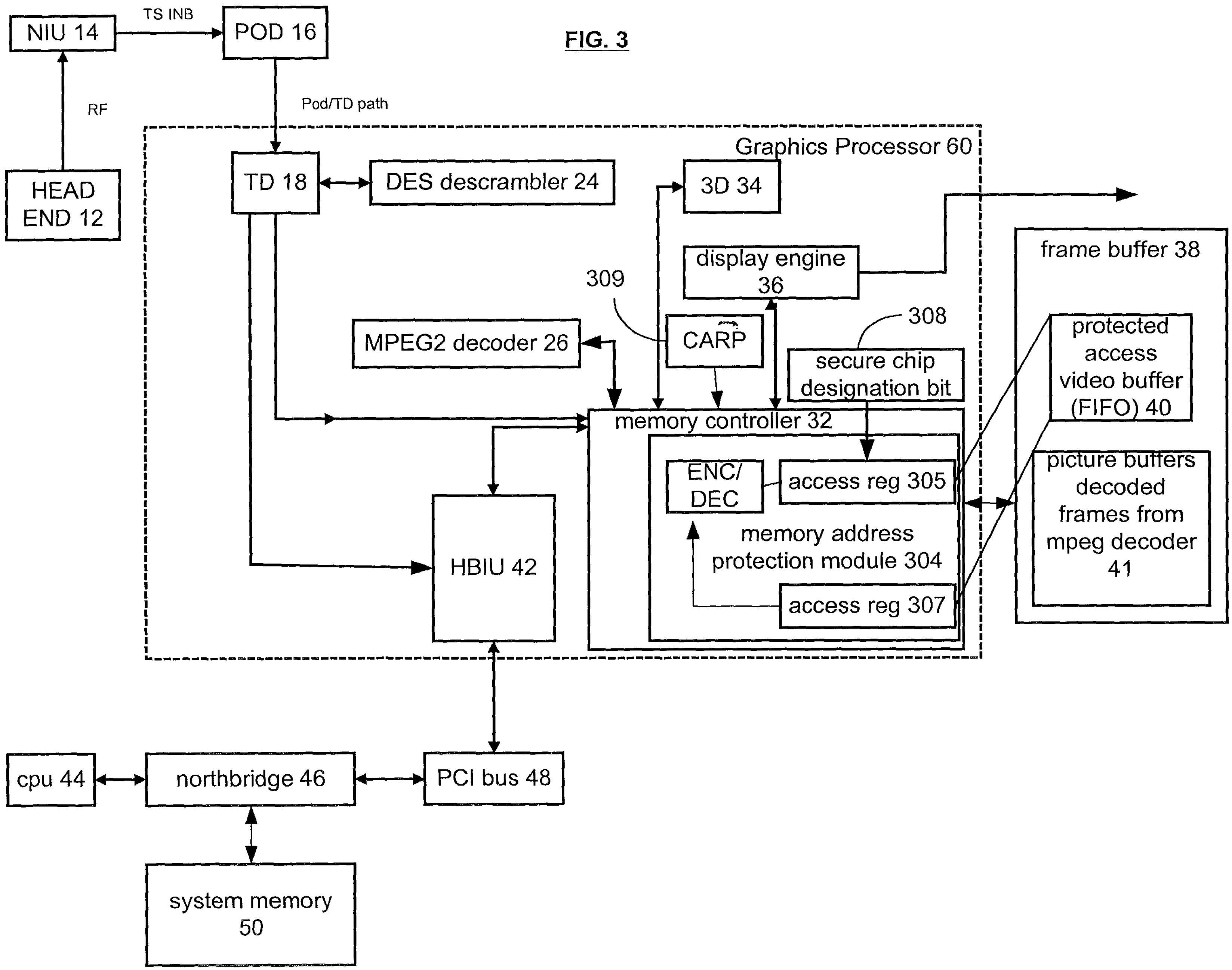
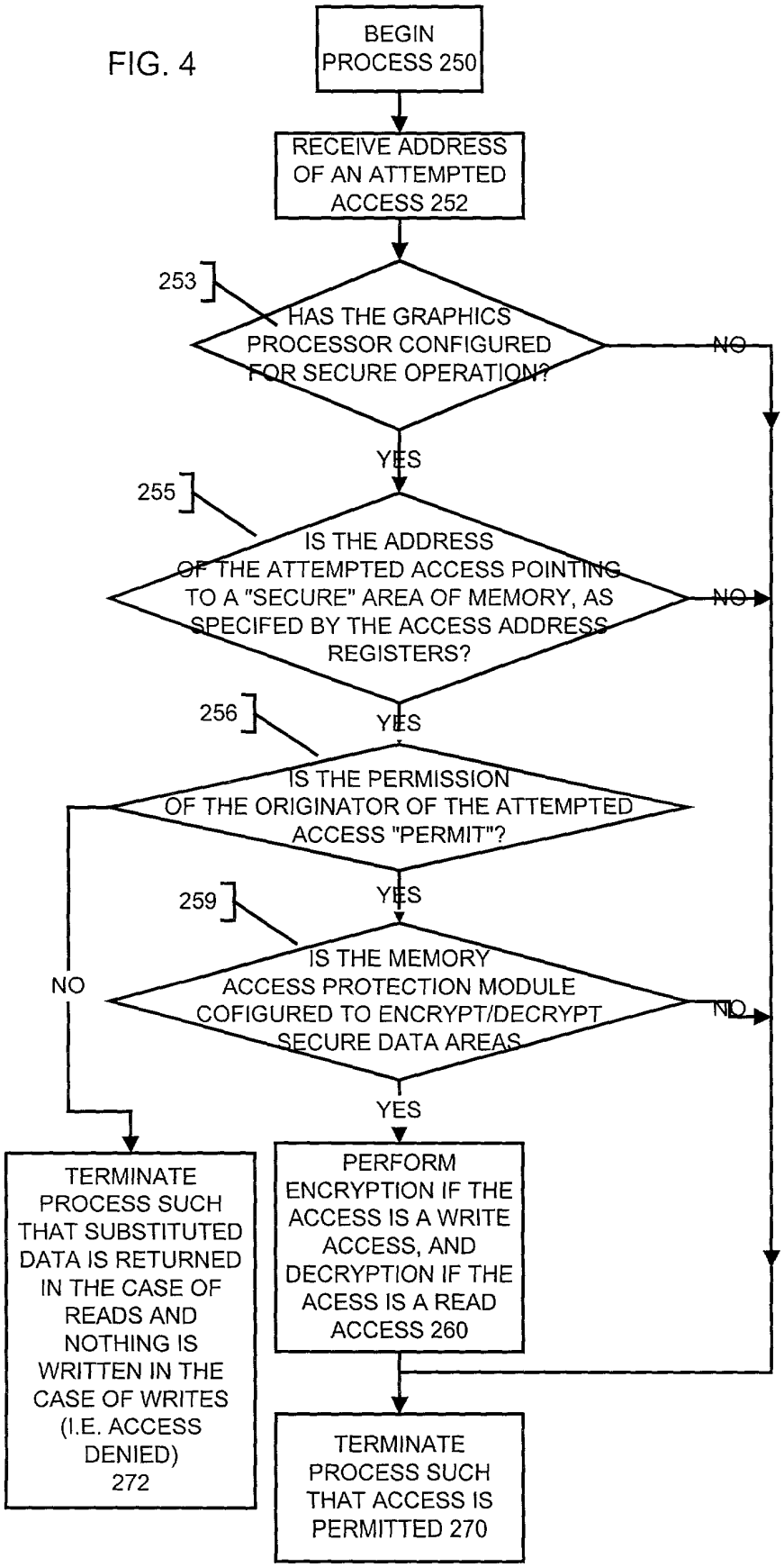

NIU 14
TS INB
POD 16
RF
HEAD END 12
Pod/TD path
Graphics Processor 60
TD 18
DES descrambler 24
3D 34
display engine 36
309
CARP
MPEG2 decoder 26
308
secure chip designation bit
memory controller 32
ENC/ DEC
access reg 305
memory address protection module 304
access reg 307
HBIU 42
frame buffer 38
protected access video buffer (FIFO) 40
picture buffers decoded frames from mpeg decoder 41
cpu 44
northbridge 46
PCI bus 48
system memory 50

FIG. 4


BEGIN PROCESS 250
RECEIVE ADDRESS OF AN ATTEMPTED ACCESS 252
253
HAS THE GRAPHICS PROCESSOR CONFIGURED FOR SECURE OPERATION?
NO
YES
255
IS THE ADDRESS OF THE ATTEMPTED ACCESS POINTING TO A "SECURE" AREA OF MEMORY, AS SPECIFED BY THE ACCESS ADDRESS REGISTERS?
NO
256
YES
IS THE PERMISSION OF THE ORIGINATOR OF THE ATTEMPTED ACCESS "PERMIT"?
259
YES
IS THE MEMORY ACCESS PROTECTION MODULE COFIGURED TO ENCRYPT/DECRYPT SECURE DATA AREAS
NO
NO
YES
TERMINATE PROCESS SUCH THAT SUBSTITUTED DATA IS RETURNED IN THE CASE OF READS AND NOTHING IS WRITTEN IN THE CASE OF WRITES (I.E. ACCESS DENIED) 272
PERFORM ENCRYPTION IF THE ACCESS IS A WRITE ACCESS, AND DECRYPTION IF THE ACESS IS A READ ACCESS 260
TERMINATE PROCESS SUCH THAT ACCESS IS PERMITTED 270